Module 2

FET and SCR

Introduction, JFET: Construction and operation, JFET Drain Characteristics and parameters, JFET Transfer chacteristics, Square law expression for I_D, Input resistance, MOSFET: Depletion and Enhancement type MOSFET-Construction, Operation, Characteristics and Symbols, CMOS
Silicon Controlled Rectifier(SCR)-Two Transistor model, Switching action, Characteristics, Phase Control application

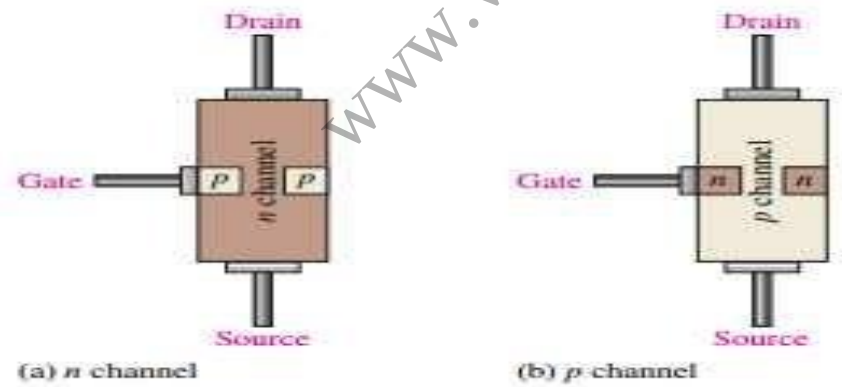
Introduction

A field effect transistor (FET)is a voltage operated device that can be used in amplifiers and switching circuits. There are two major categories of FET's Junction FET(JFET) and Metal oxide semiconductor FET(MOSFET). These are further subdivided into p-channel and n-channel devices.

JFET: Construction

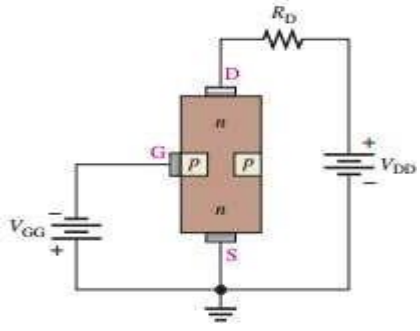
A JFET is a type of FET that operates with a reverse biased pn junction to control current in a channel. Depending on their structures, JFETs fall into either of two categories, n channel or p channel.

Fig(a) shows basic structure of an n-channel JFET. Wire leads are connected to each end of the n-channel; drain is at the upper end and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, both p-type regions are connected to the gate lead. A p-channel JFET is shown in fig(b).



(a) *n* channel (b) *p* channel

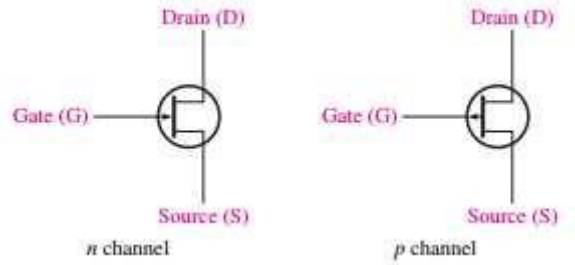
Operation



A biased *n*-channel JFET.

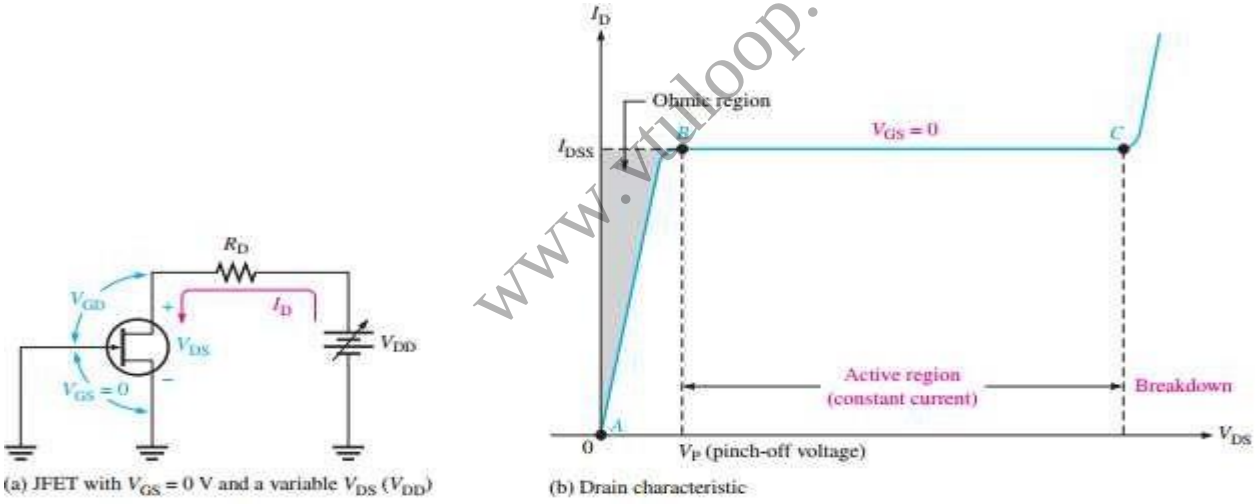
To illustrate the operation of a JFET, fig shows dc bias voltages applied to an n-channel device.V_{DD} provides a drain to source voltage and supplies current from drain to source.V_{GG} sets the reverse bias voltage between the gate and the source as shown. JFET is always operated with gate source pn junction reverse biased. Reverse biasing of the gate source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by restricting the channel width. The channel width and channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current I_D.

JFET Symbols



JFET Drain Characteristics and Parameters

Drain Characteristics curve



Consider the case when the gate-to-source voltage is zero(V_{GS}=0V)This is produce by shorting the gate to source, as in fig(a) where both are grounded. As V_{DD} is increased from 0V,I_D will increase proportionally as shown in the graph of fig(b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called ohmic region because V_{DS} and I_D are related by ohm's law.

At point B in fig(b),the curve levels off and enters the active region where I_D becomes essentially constant. As V_{DS} increases from point B to Point C, the reverse bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}. Thus keeping I_D relatively constant.

Pinch-off-voltage

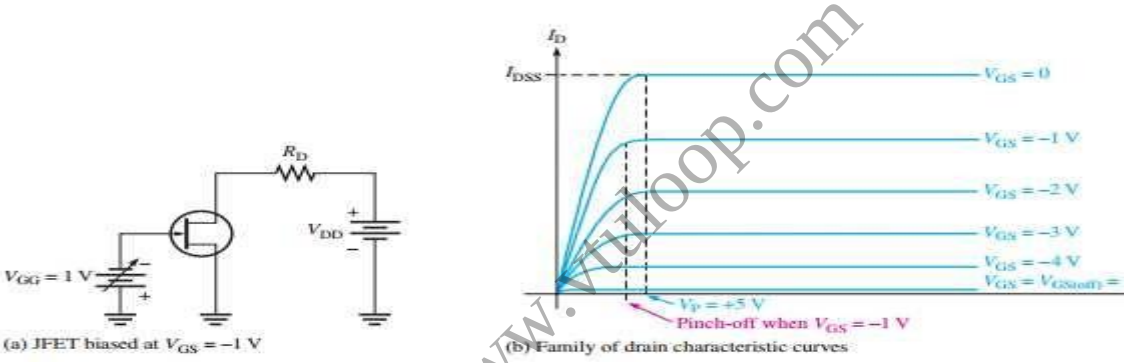
For V_{GS} =0 V, the value of V_{DS} at which I_D becomes essentially constant (point *B* on the curve in Figure (b)) is the **pinch-off voltage**, V_P. For a given JFET, *V*P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET datasheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, V_{GS}= 0 V.

Breakdown

As shown in the graph in Figure (b), **breakdown** occurs at point *C* when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points *B* and *C* on the graph).

V_{GS} Controls I_D

JFET action that produces the characteristic curve for $V_{GS} = 0$ V.



Let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure(a). As V_G is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure (b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P. The term *pinch-off* is not the same as pinchoff voltage, *V*p. Therefore, the amount of drain current is controlled by V_{GS}

Cut off Voltage

The value of V_{GS} that makes I_D approximately zero is the **cut off voltage,** V_{GS}(off),.The JFET must be operated between V_{GS}= 0 V and V_{GS}(off). For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

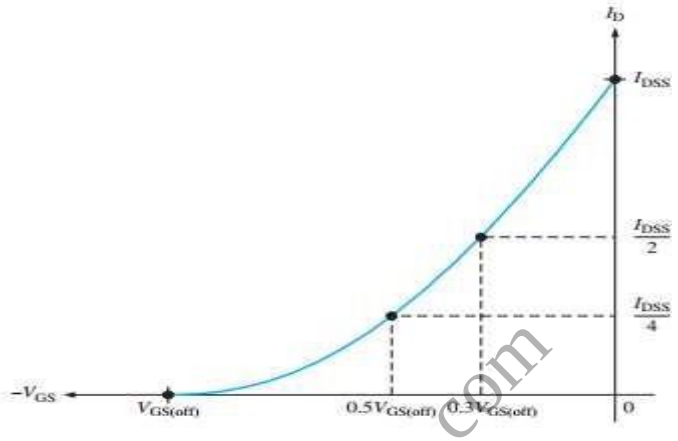
Comparison of Pinch-Off Voltage and Cut off Voltage

As we seen, there is a difference between pinch-off and cut off voltages. There is also a connection. The pinch-off voltage V_P is the value of V_{DS} at which the drain current becomes constant and equal to I_{DSS} and is always measured at V_{GS} = 0 V. However, pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes

constant varies with V_{GS}. V_{GS}(off) and V_P are always equal in magnitude but opposite in sign. A datasheet usually will give either V_{GS}(off) or V_P, but not both. However, when you know one, you have the other. For example, if V_{GS}(off) = -5 V, then V_P = +5 V, as shown in Figure (b).

JFET Transfer Characteristic

A range of V_{GS} values from zero to V_{GS}(off) controls the amount of drain current. For an *n*-channel JFET, V_{GS}(off) is negative, and for a *p*-channel JFET, V_{GS}(off) is positive. Because *V*GS does control I_D, the relationship between these two quantities is very important. Figure is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D. This curve is also known as a transconductance curve.



Notice that the bottom end of the curve is at a point on the V_{GS} axis equal to V_{GS}(off),and the top end of the curve is at a point on the I_D axis equal to I_{DSS}. This curve shows that

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{4} \quad \text{when } V_{GS} = 0.5V_{GS(off)}$$

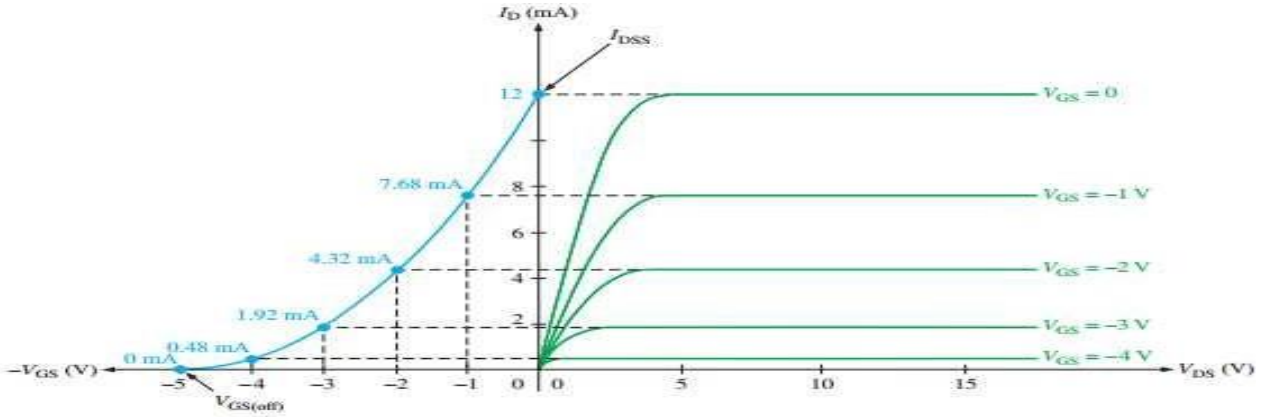
$$I_D = \frac{I_{DSS}}{2} \quad \text{when } V_{GS} = 0.3V_{GS(off)}$$

and

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off, as illustrated in Figure for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves.

For example, when V_{GS} = -2V, I_D = 4.32 mA. Also, for this specific JFET, V_{GS}(off) = -5 V and I_{DSS} = 12 mA.



Square Law Expression for I_D

A JFET transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \quad \text{---------- (1)}$$

With Equation (1), I_D can be determined for any V_{GS} if $V_{GS}(off)$ and I_{DSS} are known. These quantities are usually available from the datasheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a **square law**, and therefore, JFETs and MOSFETs are often referred to as **square-law devices**.

Input Resistance

A JFET operates with its gate-source junction reverse-biased, which makes the input resistance at the gate very high. This high input resistance is one advantage of the JFET over the BJT. (Recall that a bipolar junction transistor operates with a forward-biased base-emitter junction.) JFET datasheets often specify the input resistance by giving a value for the gate reverse current, I_{GSS}, at a certain gate-to-source voltage. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value (no sign):

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

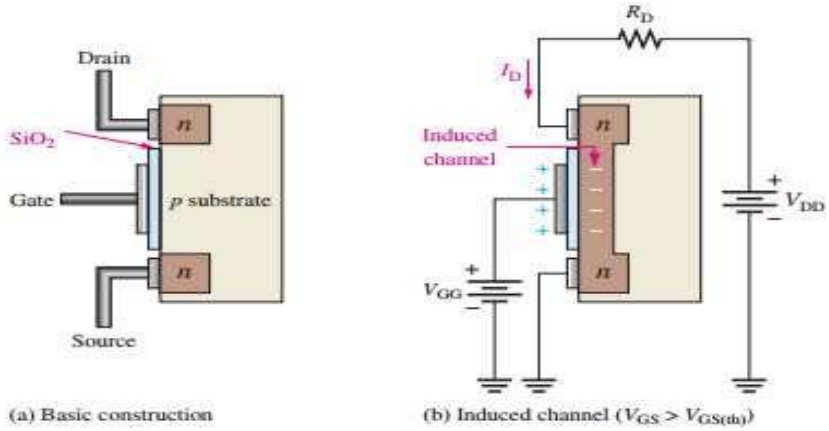
For example, the 2N5457 datasheet, maximum I_{GSS} of -1.0nA for V_{GS}=-15V at 25°C, at I_{GSS} increases with temperature, so the input resistance decreases.

MOSFET

The **MOSFET** (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET, different from the JFET, has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are enhancement (E) and depletion (D). Of the two types, the enhancement MOSFET is more widely used. Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs).

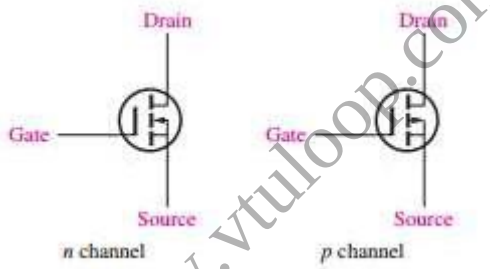
Enhancement MOSFET (E-MOSFET): Construction and Operation

The E-MOSFET operates *only* in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET, in that it has no structural channel. Notice in Figure (a) that the substrate extends completely to the SiO_2 layer. For an *n*-channel device, a positive gate voltage above a threshold value *induces* a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure (b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.



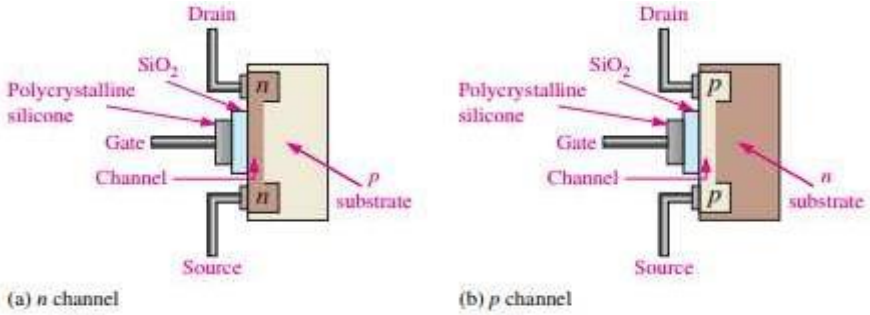
E-MOSFET Symbols

The schematic symbols for the *n*-channel and *p*-channel E-MOSFETs are shown in figure . The broken lines symbolize the absence of a physical channel. An inward pointing substrate arrow is for *n* channel, and an outward-pointing arrow is for *p* channel.Some E-MOSFET devices have a separate substrate connection.



Depletion MOSFET (D-MOSFET): Construction and operation

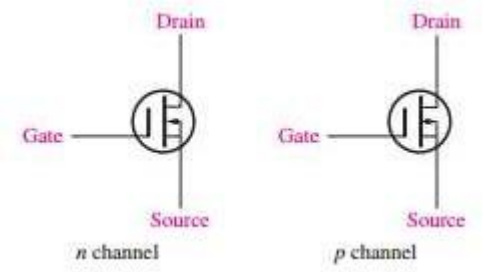
Another type of MOSFET is the depletion MOSFET (D-MOSFET), and figure illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both *n*-channel and *p*-channel devices are shown in the figure.We will use the *n*-channel device to describe the basic operation. The *p*-channel operation is the same, except the voltage polarities are opposite those of the *n*-channel.



The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode—and is sometimes called a *depletion/enhancement MOSFET*. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The *n*-channel MOSFET operates in the **depletion** mode when a negative gate-to-source voltage is applied and in the **enhancement** mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.

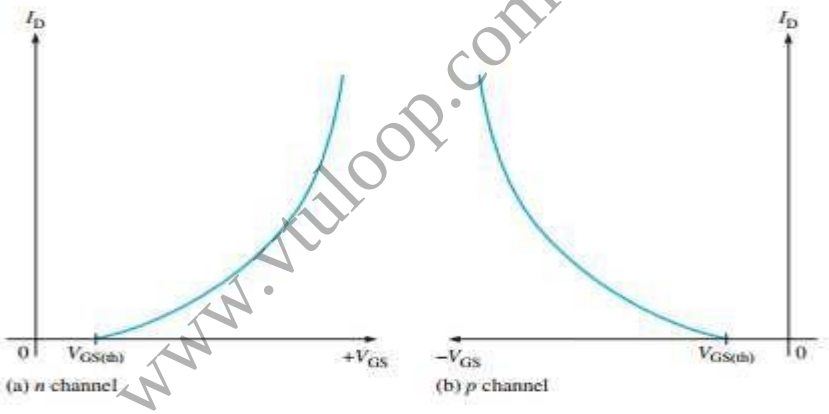
D-MOSFET Symbols

The schematic symbols for both the *n*-channel and the *p*-channel depletion MOSFETs are shown in figure. The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin.



E-MOSFET Transfer Characteristic

The E-MOSFET uses only channel enhancement. Therefore, an *n*-channel device requires a positive gate-to-source voltage, and a *p*-channel device requires a negative gate-to-source voltage. Figure shows the general transfer characteristic curves for both types of E-MOSFETs. As we see, there is no drain current when V_{GS}= 0. Therefore, the E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET. Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the ***threshold voltage***, V_{GS}(th).



The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at V_{GS}(th) rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E-MOSFET transfer characteristic curve is

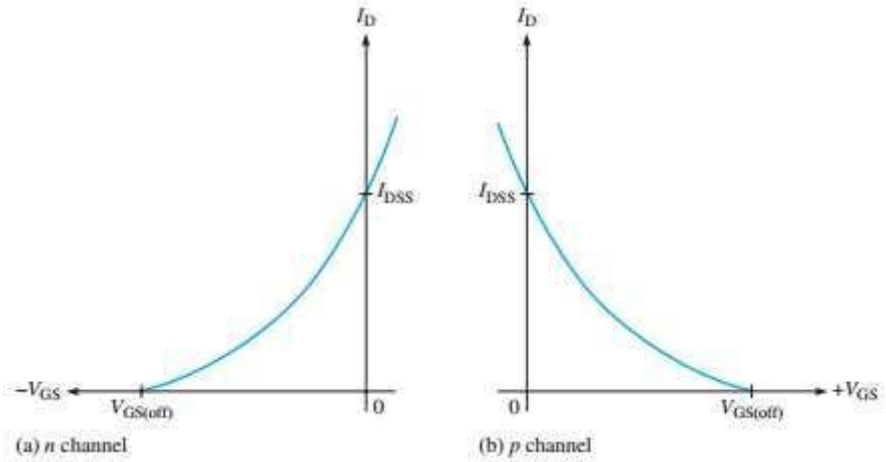
$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant *K* depends on the particular MOSFET and can be determined from the datasheet by taking the specified value of I_D, called $I_{D(on)}$, at the given value of V_{GS}

D-MOSFET Transfer Characteristic

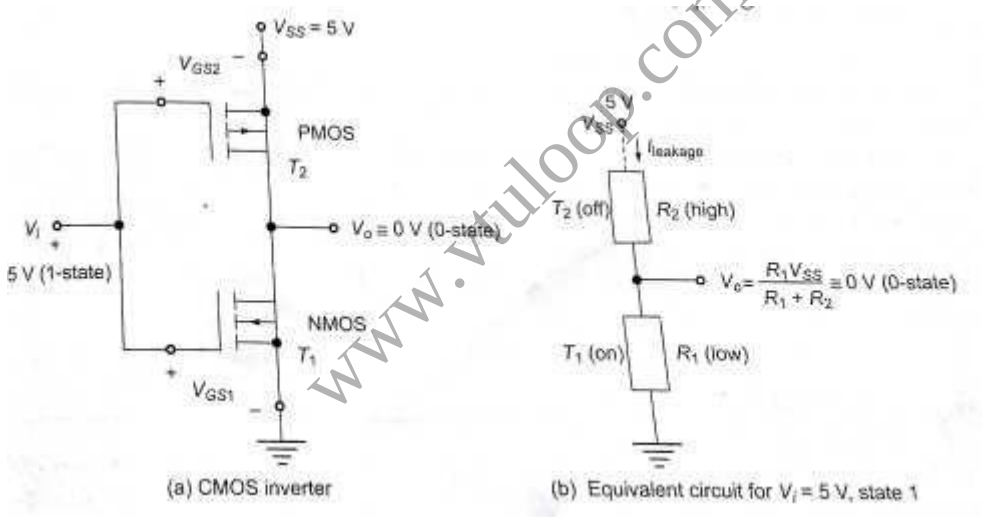
The D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure 8–45 for both *n*-channel and *p*-channel MOSFETs. The point on the curves where V_{GS} =0 corresponds to I_{DSS}. The point where I_D= 0 corresponds to $V_{GS(off)} = -V_P$.

As with the JFET, The square-law expression in Equation (1) for the JFET curve also applies to the D-MOSFET curve,



CMOS

CMOS is the complementary metal oxide semiconductor, where in two enhancement MOSFET's, one N-type(NMOS) and other P-type(PMOS),are connected as a complementary pair. The two gates are connected to form the input terminal and the two drains are connected to form the output terminals as shown in fig(a).



The CMOS circuit offers two advantages:

1. The drain current is very low and flows mainly during transition from one state to the other (ON/OFF).
2. The power drawn in steady state is extremely small.

Digital Circuit Applications

The circuit for a CMOS digital inverter is as in fig(a).The source terminal of PMOS (T_2) is connected to V_{ss}=5V,while the source terminal of NMOS(T_1)is grounded.

Operation

1. **Input**

V_i=5V 1-state

V_{GS}=5-5=0V

T_2 is nonconducting, OFF (its V_T is negative),draws only leakage current, offers high resistance (R_2)

V_{GS1}=5V>V_T

T_1 is conducting, ON offers very low resistance(R_1).The circuit equivalent in this state is drawn in fig(b)

Output $V_0=0$ 0-state

It can be seen from the circuits of fig(b) that

$V_O=(R_1/R_1+R_2)V_{SS}$ =0V

2.Input

V_i=0V 0-state

V_{GS2}= -5V , T_2 is conducting(low resistance)

V_{GS1}= -5V , T_1 is non conducting(high resistance)

Output

V_0=5V 1-state

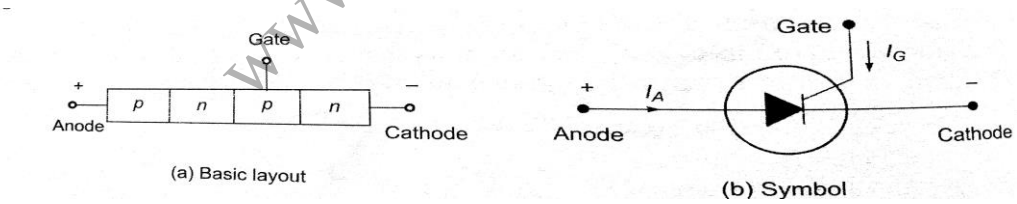
Thus we can see that the circuit acts as an inverter;1-state input produces 0-state output and 0-state input produces 1-state output.

Silicon Controlled Oscillator(SCR)

It is a four layer device which along with its associated circuitry has a very wide range of applications-Rectifiers, Regulated power supplies,DC to AC conversion, Relay Control,Time Delay circuits and many more.

Basic Operations and Symbols

The material used for SCR is silicon because of high temperature requirement of handling large current and power. Its four layers are arranged as pnpn shown in fig. The outer layers are connected to terminals to form **Anode** (positive terminal) and **Cathode** (negative terminal).The P-layer closer to the cathode is connected to the gate terminal. The SCR symbol is drawn in fig.It is similar to that of diode, the difference being the indication of the gate terminal.

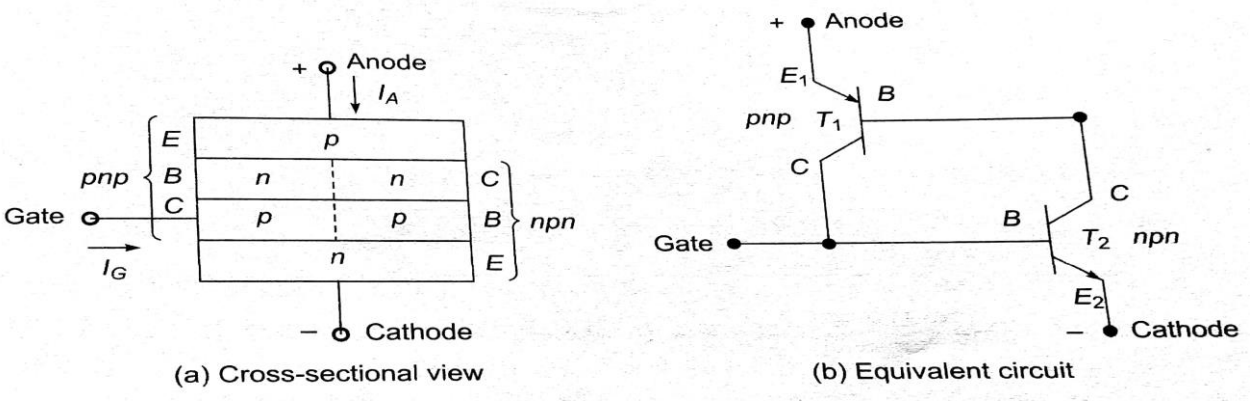


As a forward voltage is applied across the anode(+) and cathode(-),no conduction takes place as the middle np junction is reverse biased. If a positive pulse is applied at the gate, such that a current of magnitude equal to more than I_G, (turn-on)flows into the gate, the processes in the device cause it to go into conduction. The forward current (anode to cathode) is offered a resistance as 0.01 to 0.1Ω.However, because of regenerative action, removing the gate current does not cause the device to turn off. The dynamic reverse resistance of an SCR is as high as 100KΩ or more.

Two Transistor Model

The cross sectional view of an SCR with its four layers is drawn in fig. The device comprises one PNP and one NPN transistor. The base of PNP is connected to the collector of NPN, and the collector of PNP is connected to the base of NPN, while gate is connected to the base of NPN.

The corresponding two transistor model equivalent circuit is drawn in fig.



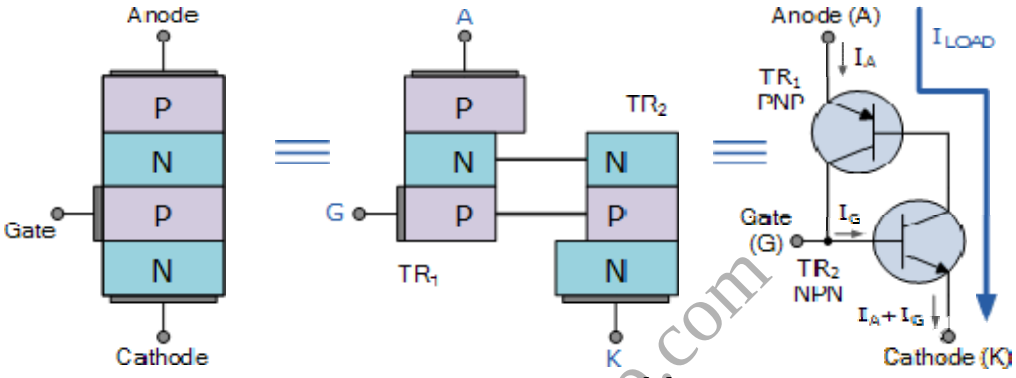


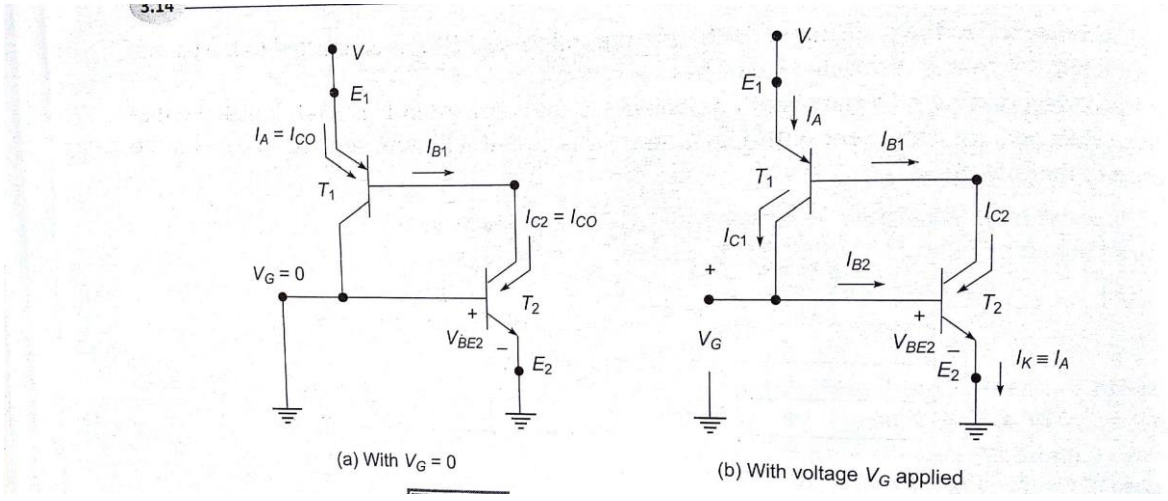
Fig: Two transistor model

Switching Action

Let a positive V is applied to the anode (E_1),and the cathode (E_2) and gate(G) be both grounded as shown in fig(a). As $V_G=V_{BE2}=0$, the transistor T_2 is in 'off' state. It means that CB junction of T_2, through EB-junction of T_1 is reverse biased. Therefore, $I_{B1}=I_{CO}$(minority carrier current)is too small to 'turn – on'T_1.Thus T_1 and T_2 are 'off' and so anode current.

$$I_A= I_{B1}=I_{CO}$$

is off negligible order. It means that SCR is in 'turn-off' state, that is the switch between anode (E_1) and cathode (E_2) is open.



Now ,let a voltage $+V_G$ be applied at the gate as shown in fig(b). As $V_{BE2}=V_G$, on making V_G sufficiently large ,I_{B2} will cause T_2 to turn on and the collector and the collector I_{C2} becomes large. As

$I_{B1}=I_{C2,}T_2$ turns on causing a large collector current $I_{C1}(I_A=I_{C1})$ to flow. This in turn, increases I_{B2} causing a regenerative action to set in. The result is that the SCR is turned on, that is switch between anode(E_1) and cathode(E_2) is closed (turn-on).The current I_A must be limited by the external circuit,say a series resistance between the source and E_1.

The turn-on time of an SCR is typically 0.1 to 1µs.However,for high power devices in the range of 100-400A,turn-on time may be 10-25µs.

TURN -OFF

When the SCR is in conduction mode, the gate is ineffective in turning it off. The turn off mechanism is called **commutation** and it can be achieved in two ways

Natural commutation: When the source that feeds the current to anode of SCR is such that naturally passes through zero, the SCR turns off at the current zero. This is the case when the SCR is fed from the ac source. In this situation, the commutation is also known as line commutation.

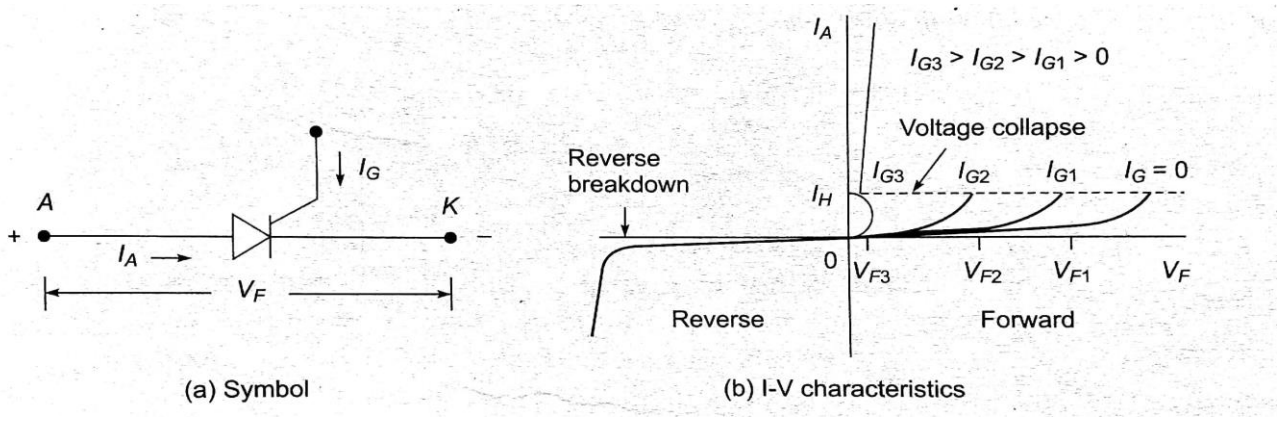
Forced commutation: In this method of commutation, the current through the SCR is forced to become zero by passing a current through it in opposite direction from an independent circuit.

Turn-off Circuit

Basic Turn-off circuit is shown in fig. A transistor and a dc battery source in series are connected to the SCR. When the SCR is in conduction mode(on),$I_B=0$ and when the transistor is off, it is almost an open circuit. To turn off the SCR, a positive I_B pulse of magnitude large enough to drive the transistor into saturation is applied at the transistor base. The transistor acts almost like a short circuit. This causes flow of very large I_{off} through the SCR in the opposite direction to its conduction current. The total SCR current reduces to zero in a very short time causing it to turn off.The transistor has to withstand a large current but for a very short time.Turn-off time of an SCR is typically 5-30µs.

SCR Characteristics

The symbol and I-V characteristics of an SCR are given in fig. Various voltages and currents which provide important information for SCR application.



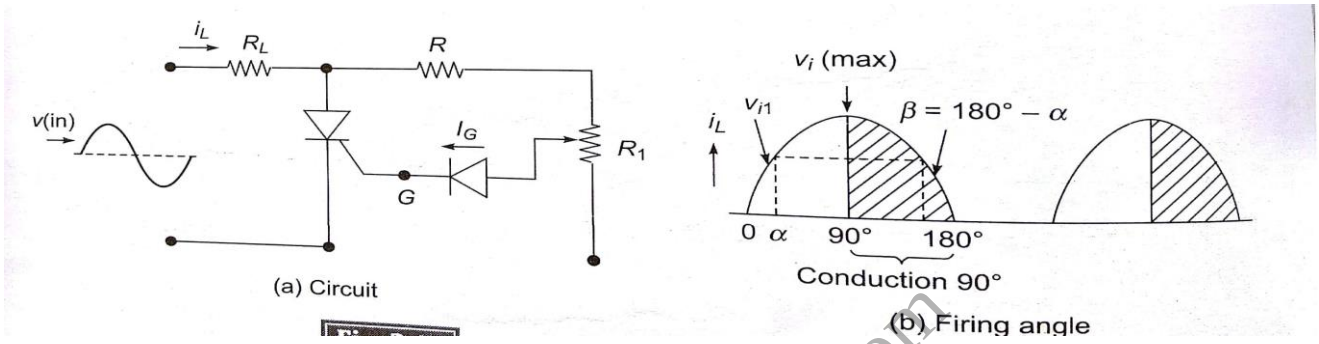
1. **Forward breakover voltage V_F (BR)** is the voltage at which for a given I_G,the SCR enters into conduction mode. As in fig, that this voltage reduces as I_G ,increases. V_F (BR) has dependence on the circuit connection between G and K terminals.
2. **Holding current I_H** is the value of the current below which SCR switches from conduction state to forward blocking regions of specified conditions.

3. **Forward and reverse blocking** regions are those regions in which the SCR is open circuited and no current flows from anode to cathode.
4. **Reverse breakdown voltage** corresponds to zener or avalanche region of a diode.

Applications of SCR

Variable Resistance Phase Control

A variable phase control circuit is as in fig. The SCR gate current is controlled through R and the variable R_1.Let R_G be adjusted to high value so that even at the peak value v_i(positive),$I_G < I_{G(turn\text{-}on)}$ and no conduction takes place. As R_1 is reduced, I_G rises to turn on the value at a particular angle(time)of v_i. The conduction then begins and continues till v_i reaches zero (180^0).Varying R_1 allows the adjust of SCR firing angle from 0^0 to 90^0 as shown in fig.



At R_1,corresponding to the firing angle of 90^0, $v_{i=}$ $v_{i(max)}$ .If R_1 is adjusted for firing angle at α,the firing will takes place at angle $\alpha < 90^0$ but not at angle $\beta=(180^0-\alpha) > 90^0$ as the angle α is reached in time on the v_i wave. So the operation of this circuit is known as **half-wave, variable –resistance phase control.**

Thus, i_L(dc) can be adjusted to the maximum value at 0^0 to the minimum value of 90^0.It may be noted that a diode is provided in the firing circuit to prevent the flow of reverse gate current.